Advanced Electronics Technologies: Challenges for Radiation Effects Testing, Modeling, and Mitigation

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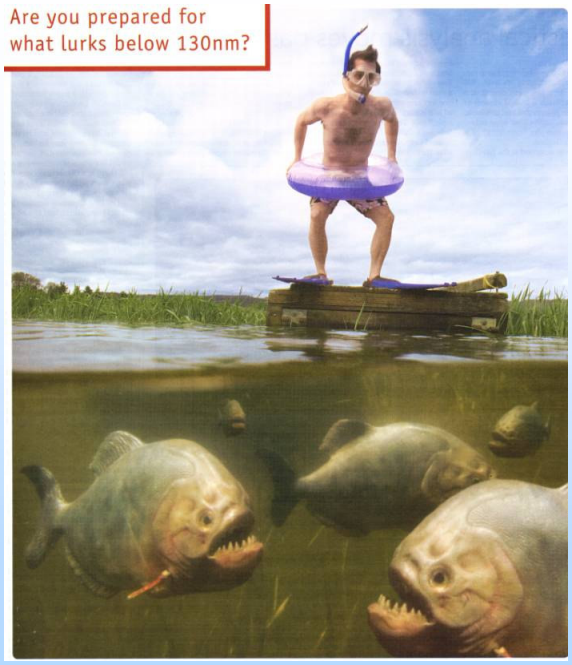
Outline

- Emerging Electronics Technologies
  - Changes in the commercial semiconductor world
- Radiation Effects Sources
  - A sample test constraint
- Challenges to Radiation Testing and Modeling
  - IC Attributes – Radiation Effects Implications
  - Fault Isolation
  - Scaled Geometry
  - Speed
  - Modeling Shortfalls
  - Knowledge Status
- Summary
- Recommendations

Notes:

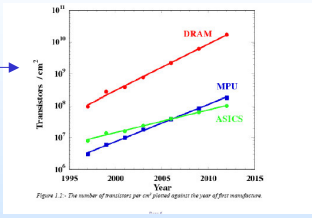
1.The emphasis of this presentation is digital technologies and SEE.

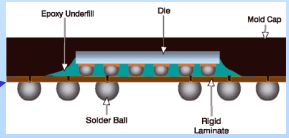
2. A discussion of mitigation implications is included in the notes.



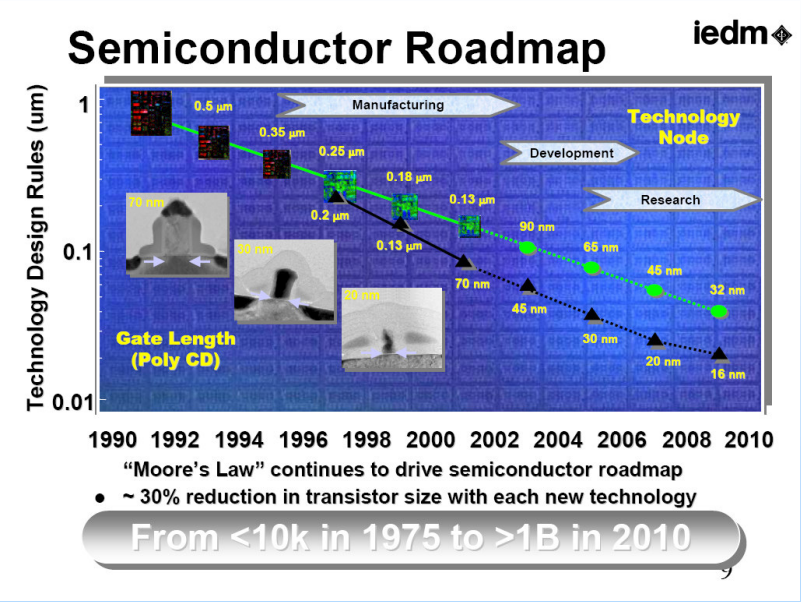
Changes in the Electronics World

- Over the past decade plus, much has changed in the semiconductor world. Among the rapid changes are:
  - Scaling of technology
    - Increased gate/cell density per unit area (as well as power and thermal densities)
    - Changes in power supply and logic voltages (<1V)
      - Reduced electrical margins within a single IC
    - Increased device complexity, # of gates, and hidden features
    - Speeds to >> GHz (CMOS, SiGe, InP…)
  - Changes in materials
    - Use of antifuse structures, phase-change materials, alternative K dielectrics, Cu interconnects (previous – Al), insulating substrates, ultra-thin oxides, etc…
  - Increased input/output (I/O) in packaging
    - Use of flip-chip, area array packages, etc
  - Increased importance of application specific usage to reliability/radiation performance

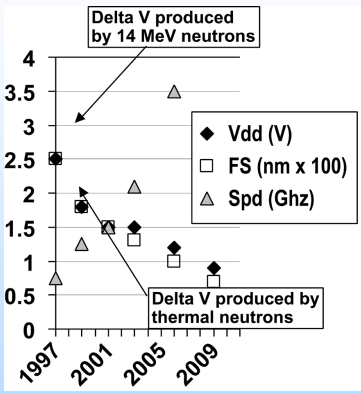




Mainstream digital – CMOS scaling



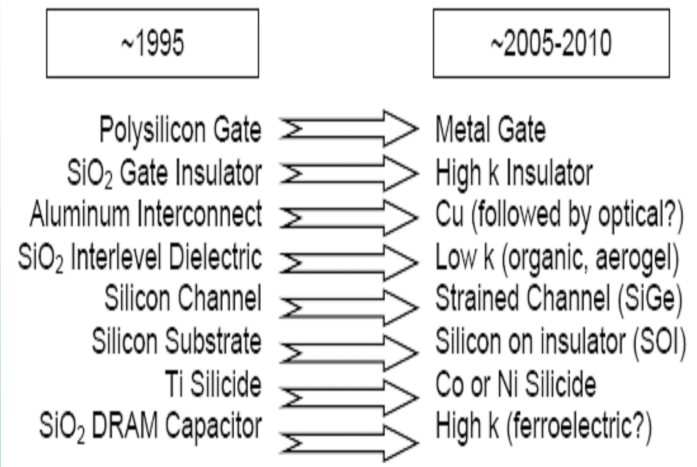
Neutron-Induced Transients vs. Feature Size (FS), Vdd, and Speed



Year	97	99	01	03	06	09
FS (nm)	250	180	150	130	100	70
Spd (Ghz)	0.75	1.25	1.5	2.1	3.5	6.0
Trans/chip µproc (M)	11	21	40	76	200	520
Vdd	2.5	1.8	1.5	1.5	1.2	0.9

Note the magnitude of the voltage transient equals or exceeds the operating voltage for circuits fabricated using 180nm technology [Mass01-van]

Changing Materials for Mainstream CMOS



Virtually all of the Materials used to fabricate IC's in 1995 will be different in 2010
A&T Dellin, 2005, 21st Century Semiconductor Technology

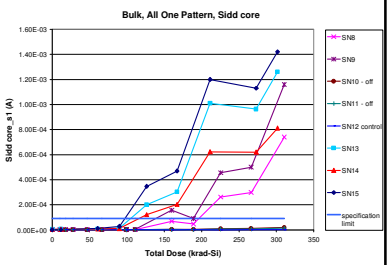
Changes in IC Attributes vs. Radiation Effects

Attributes	SEU	MBU	SET	SEFI	SEGR	TID
Intelligence	++	++	+	++	-	-
Flexibility	++	++	-	+++	-	+
Complexity	+++	-	+	-	+	++
Integration Density	+	+++	-	-	-	-
Hidden Circuit Features	+	-	-	+++	-	-
Construction	++	++	++	++	++	++
Power	+	+	++	-	-	-
Speed	-	-	+++	-	-	-

+ = worse
++ = much worse
+++ = very significant impact
- = no effect

Total Ionizing Dose – Summary trends

- Deep sub-micron (<0.25um) CMOS basic structures have shown increasing tolerance to TID (thinner oxides)
  - >100 krad(Si)
- However,
  - Complex structures and those that require higher voltage fields such as charge pumps in flash memories or FPGAs may be MUCH more TID sensitive
  - Bipolar devices do not scale as easily and are susceptible to enhanced low dose rate sensitivity (ELDRS)
    - Failure at << 100 krad(Si) at low space dose rates
    - Scaled CMOS devices observing ELDRS-like effect (Wiczak, 2005)

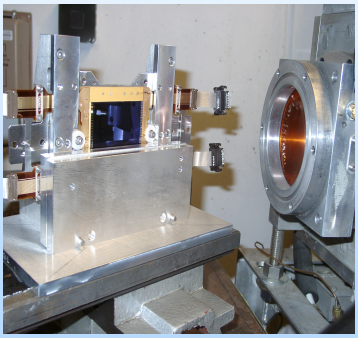


Sample Bulk CMOS 0.18um Technology Demonstrating ~ 100 krads(Si) Tolerance
Poivey 2005

Typical Ground Sources for Space Radiation Effects Testing

- Issue: TID
  - Co-60 (gamma), X-rays, Proton
- Issue: Displacement Damage
  - Proton, neutron, electron (solar cells)
- SEE (GCR)
  - Heavy ions, Cf
- SEE (Protons)
  - Protons (E>10 MeV)
- SEE (atmospheric)
  - Neutrons, protons

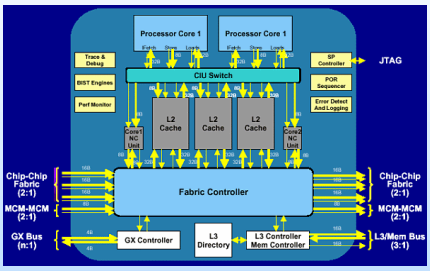
TID is typically a local source with nearby ATE. All others require travel and shipping
- A constraint for how testing is done.



Wide Field Camera 3 E2V
2k x 4k n-CCD in front of Proton Beam at UCDavis

Radiation Test Challenge – Fault Isolation

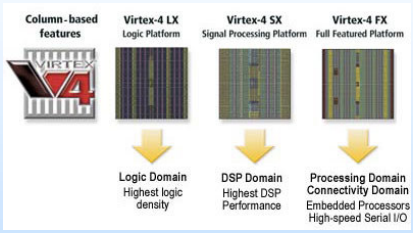
- **Issue: understanding what within the device is causing fault or failure.**
  - **Identification of a sensitive node.**
- **Technology complications**
  - **"Unknown" and increased control circuitry (hidden registers, state machines, etc..)**
    - **Monitoring of external events such as an interrupt to a processor limits understanding of what may have caused the interrupt**
      - **Example: DRAM**
        - » **Hits in control areas can cause changes to mode of operation, blocks of errors, changes to refresh, etc…**
      - **Not all areas in a device are testable**



Power4 Processor Architecture

Fault Isolation –(2)

- **Example: SRAM-based reprogrammable FPGA-measuring sensitivity of user-defined circuit**
  - **SEE in configuration area corrupts user circuitry function**
    - **Can cause halt, continuous misoperation, increased power consumption (bus conflicts), etc.**
  - **Often the sensitivity of the configuration latches overwhelm user circuitry sensitivity**
    - **Must have correct configuration to measure user circuit performance**
- **Increased number of control structures in a device drives an increasing rate of single event functional interrupts (SEFIs)**



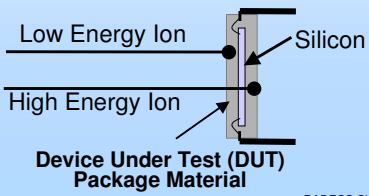
Complex new FPGA architectures include hard-cores: processing, high-speed I/O, DSPs, programmable logic, and configuration latches

Potential SEU Sites in a SRAM-based FPGA

Chip Area	SEE Issue	Possible SEU Mitigation
Config. Memory	Single and multiple bit errors corrupting circuit operation, causing bus conflicts (current creep), etc…	• Scrubbing • Partial reconfiguration
Config. Controller	Improper device configuration can occur if hit during configuration/reconfiguration	• Partitioned design • Multiple chip voting (Redundancy by using multiple devices)
CLB	Logic hits and propagated upsets caused by transients	• Triple modular redundancy (TMR) • Acceptable error rates
BRAM	Memory upsets in user area	• TMR • Error Detection and Correction (EDAC) scrubbing
Half-latches	Sensitive structure used in configuration/routing	• Removal of half-latches from design
POR	SEUs on POR can cause inadvertent reboot of device	• Multiple chip voting (Redundancy by using multiple devices)
IOB	SEUs can cause false outputs to other devices or inputs to logic	• Leverage Immune Config. Memory cell • Evaluate input SET propagation
DCM	Can cause clock errors that spread across clock cycles	• TMR • Temporal TMR
DSP	Hard IP that is unhardened that can cause single event functional interrupts (SEFIs) or data errors	•TMR •Temporal TMR
MGT	Gigabit transceivers. Hits in logic can cause bursts or SEFIs. O/w bit errors in data stream	• TMR • Protocol re-writes
PPC	Hard IP that is unhardened. SEFIs are prime concern	• TMR or software task redundancy
SEL	Higher current condition that is potentially damaging	• No mitigation other than substrate addition (epi). • Circumvention techniques possible

Fault Isolation –(3)

- **Macrobeam structure: implies probabilistic chance of hitting a single node that may be sensitive**
  - **If test is run for SEE, typical heavy ion test run is to 1x 10^7 particles/cm^2.**
    - **Ex., SDRAM – 512 Mb (5x10^8 bits plus control areas)**
      - **If all memory cells are the same, no issue. BUT if there are weak cells how do you ensure identifying them?**
      - **Control logic may be a very small area of the chip. If you fly 1000 devices, area is no longer "small"**
  - **Difficult to evaluate clock edge sensitivity of a node**
- **Die access (required for most single event testing)**
  - **Typical heavy ion single event macrobeam simulators have limited energy range**
    - **Implies limited penetration through packaged device**
    - **Access to die typically required**
      - **Overlayers, metalization, etc must be taken into account**

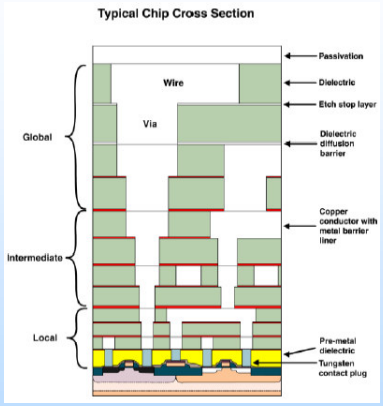


Facility	Ion (Energy)	LET (Si)	Range in Si (μm)	Peak LET
NSCL	Xe (3.2 GeV)	40	272	69
TAMU	Ar (2 GeV)	5.9	390	18

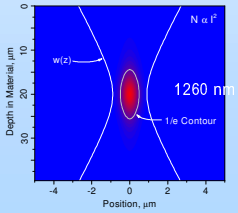
Table assumes ion traverses 1.5 mm plastic; LET given in MeV-cm^2/mg

Fault Isolation –(4)

- **Standard microbeam and laser test facilities have similar limitations for range of particle**
  - **On older technologies, these facilities are used to determine what structure within a device is causing fault/failure**
  - **New technique (two-photon absorption - TPA) with the laser is being developed, but is still in research phase**
  - **New test structures built specifically for test may be required**
    - **Reduced metalization, special packaging, etc.**

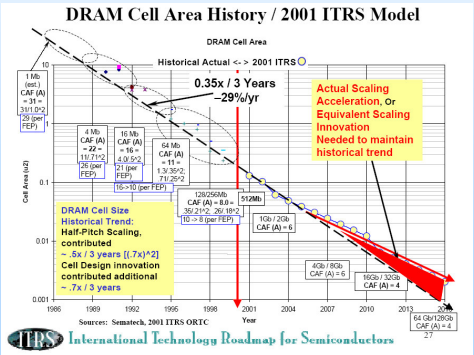


TPA is a new technique to overcome some of the test limitations from packaged device and metalization issues.
Courtesy Dale McMorrow, NRL



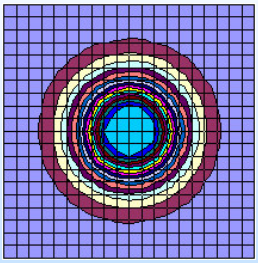
Radiation Test Challenge – Geometry

- **Issue: the scaling of feature size and closeness of cells**
- **Technology complications**
  - **Multiple node hits with a single heavy ion track**
    - **Because of the closeness of transistors and thinness of the substrate material, a single particle strike can effect multiple nodes potentially defeating hardening schemes.**



Geometry Implications (2)

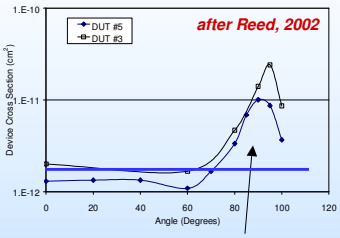
- Multiple node hits (cont'd)
  - Ex., memory array
    - A single particle strike can spread charge to multiple cells. If the cells are logically as well as physically located
      - Standard memory scrub techniques such as Hamming Code can be defeated
    - This is not new, simply exacerbated by scaling. Traditional SEU modeling considers particle strikes directly on a transistor
  - Charge spreading for strikes near but not on the transistor can generate errors
    - Measured error cross-sections may exceed physical cross-sections
  - Albeit actual individual targets are smaller for a single particle
    - More targets and the spread of non-target hits implied potentially increased error rates per device
  - The role of particle directionality and of secondaries requires future use of physics-based particle interaction codes coupled with circuit tools.
    - GEANT4, MCNPX, etc. are the type of codes required
      - Efforts begun to turn these into tools and not just science codes



Charge spreading from a single particle in an active pixel sensor (APS) array impacts multiple pixels

Geometry Implications (3)

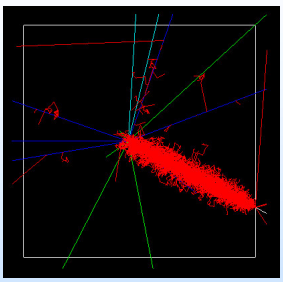
- High-aspect ratio electronics
  - For "standard" devices, the direction of the secondary particles produced from a proton (or neutron) are considered omnidirectional
  - However, for electronics where there is a high-aspect ratio (very thin with long structure), this is not the case
    - The forward spallation of particles when the proton enters the device along the long structure increases the potential error measurement cross-section
    - Test methods and error rate predictions need to consider this



Effects of protons in SOI with varied angular direction of the particle; Blue line represents expected response with "standard" CMOS devices.

Geometry Implications (4)

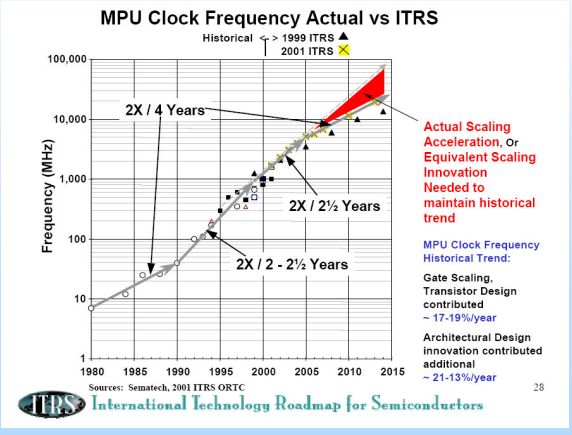
- Ultra-thin oxides provide two concerns
  - Single particles rupturing the gate
    - This is a function of the thinness and the current across a gate oxide
  - The impact of oxide defects
    - Role for TID
- Secondaries from packaging material
  - Even on the ground, particle interaction with packaging materials can cause upsets to a sensitive device
    - Ex., Recent FPGA warning of expectation of up to 1 upset/spontaneous reconfiguration a day!
- Small probability events have increased likelihood of occurring
  - If 1 in a 10^9 particles causes a "larger" LET event or 1 in 10^6 transistors can cause a more complex error
    - With billion plus transistor devices and potential use of >1000 of the same device (re: solid state recorders), small probabilities become finite



Sample 100 MeV proton reaction in a 5 um Si block. Reactions have a range of types of secondaries and LETs. *(after Weller, 2004)*

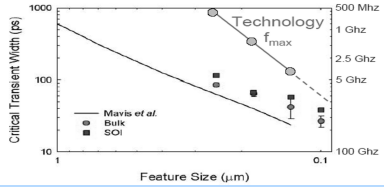
Radiation Test Challenge – Speed Implications

- Issue: the increasing device speeds (>> GHz) impact testing, test capability requirements, and complicate effects modeling.

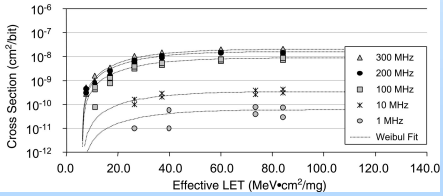


Speed (2)

- **Technology Complications**
  - **Propagation of single event transients (SETs)**
    - **As opposed to a direct upset by a particle strike on a latch-structure, the particle hit causes a transient (think hit on a combinatorial logic or such) that can propagate to change the state of a memory structure down the chain.**
      - **The transient pulse width can be on the order of picoseconds to nanoseconds (or longer depending on circuit response)**
        - » **Older, slower devices didn't recognize the transient (I.e., minimum pulse width required for circuit response was greater than that generate by a single particle)**
        - » **Newer devices can now respond to these hits increasing circuit error rates**
      - **Transient size in analog devices has been seen to be a partial function of the range of the particle entering the device**
        - » **Impacts facility usage choices**



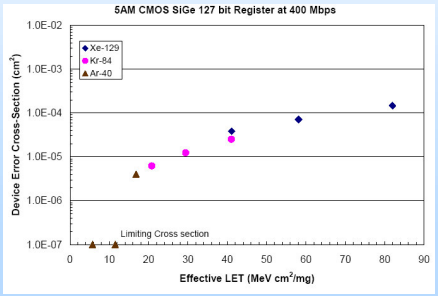
Critical width for unattenuated propagation of SETs decreases with feature size, ***Dodd-04***

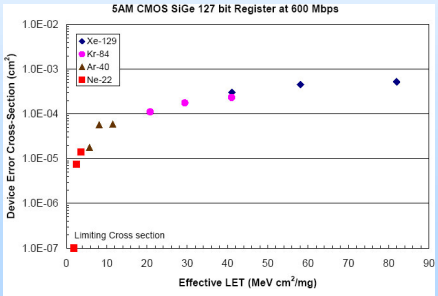


DSET for 0.18 um vs Freq ***Benedetto-04***

Speed (3)

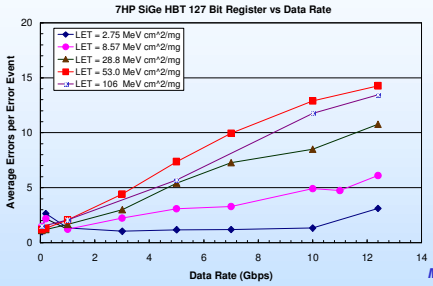
- **Propagation of SETs (cont'd)**
  - **Crossover appears in the ~400-500 MHz regime**
    - **Charge generation can now last for multiple clock cycles**
      - **Impact is to defeat hardening schemes that assume only a single clock cycle is affected**

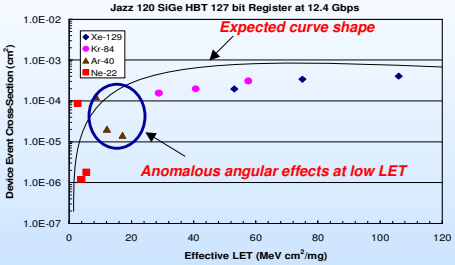




Marshall-04

Speed (4)





Marshall-04

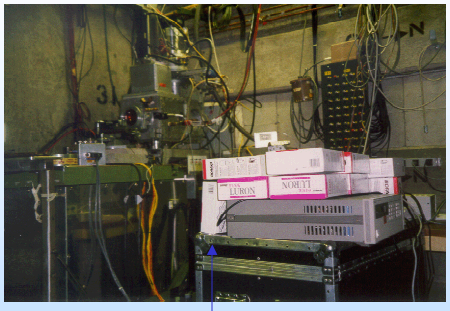
Average number of errors noted by a single particle event increases with speed and LET

Effects of heavy ions on SiGe devices at 12 GHz speeds notes anomalous charge collection of this high-speed technology; Drawn line represents expected response with "standard" models.

Speed (5)

Testing at a remote facility requires highly portable test equipment capable of high-speed measurements

- **Tester needs to be near the device or utilize high-speed drivers**
  - **Cable runs between the device under test (DUT) and the tester can be up to 75 feet**
- **Simple devices like a shift register chain can be tested using bit error rate testers (BERTs)**
  - **BERTs can run to ~$1M and tend to be very sensitive to problems from shipping**
    - **At proton test facilities secondaries are generated (neutrons) that can cause failures in the expensive test equipment if they are located near the DUT**
- **Self-test techniques for testing devices being developed for shift-registers**
  - **Modern reconfigurable FPGA-based test boards being developed to test more generic devices**



Beware of stray neutrons impinging on your test equipment.
Here, Borax is shown on top of a power supply to absorb neutrons.

Speed (6)

- **Testing in a vacuum chamber implies mechanical, power/thermal, and hardware mounting constraints**
  - **High-speed devices often mean high power consumption**
    - **Issue is mounting of DUT in vacuum chamber and removal of thermal heat**
      - **Can also be a challenge NOT in a vacuum**
      - **DUT may need to be custom packaged to allow for thermal issues**
    - **Active system required for removal of heat**

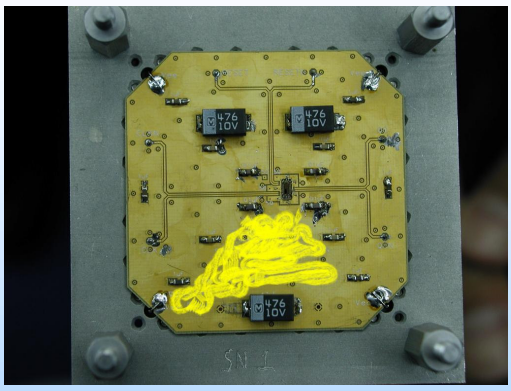
Brookhaven National Laboratories' Single Event Upset Test Facility (SEUTF)

Vacuum Chamber

User equipment area

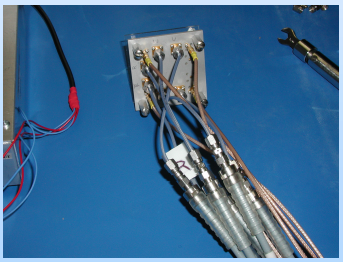
Specialty Packaging for Radiation Test

- *Thermal, Speed, Power*

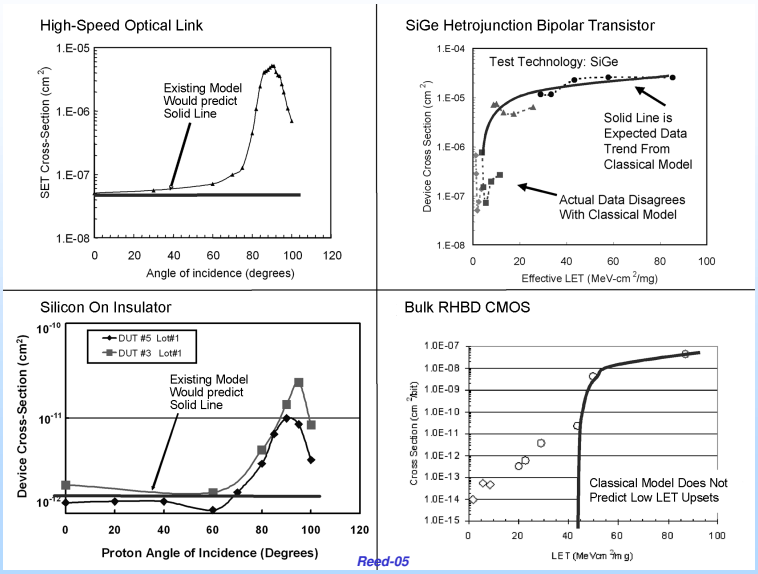


Front

Back



Sample Modeling Shortfalls



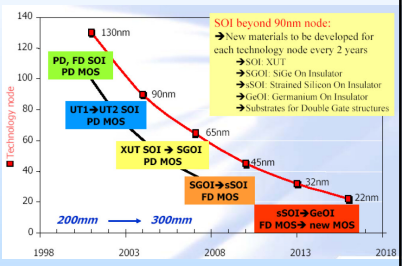
Reed-05

Radiation Status for Advanced Electronics

Radiation Response	Guideline Document	Test Method	Data Base	Modeling & Simulation
SEU/MBU	Yes	Yes	Yes	~ mature
SET	No	No	No	No
SEL	Yes	Yes	Yes	No
SEGR	No	No	No	No
SEFI	No	No	No	No
TID	Yes	Yes	Yes	Yes
Displacement Damage	Yes	Yes	No	No

Summary and Comments

- We have presented a brief overview of SOME of the radiation challenges facing emerging scaled digital technologies
  - Implications on using consumer grade electronics
  - Implications for next generation hardening schemes
- Comments
  - Commercial semiconductor manufacturers are recognizing some of these issues as issues for terrestrial performance
    - Looking at means of dealing with soft errors
  - The thinned oxide has indicated improved TID tolerance of commercial products
    - Hardened by "serendipity"
      - Does not guarantee hardness or say if the trend will continue
    - Reliability implications of thinned oxides



Next Generation SOI:
Weak or no body ties will not solve SEU problems

The Top Five Research/Development Areas Required for Radiation Test and Modeling – Author's Opinions

- 5 Understanding extreme value statistics as it applies to radiation particle impacts
- 4 System Risk Tools
- 3 High-Energy SEU Microbeam and TPA Laser
- 2 Portable High-Speed Device Testers
- 1a Physics Based Modeling Tool
- 1b Development of substrate engineering processing methods to decrease charge generation and enhance recombination